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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,518	11/02/2001	Terence R. Klein	068363.0113	4693

			EXAMINER
31625	7590	08/25/2004	JORGENSEN, LELAND R

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ART UNIT	PAPER NUMBER
2675	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

	Application No.		Applicant(s)
Office Action Summary	10/004,518		KLEIN ET AL.
	Examiner		Art Unit
	Leland R. Jorgensen		2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 November 2001</u>.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1 - 25</u> is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) <u>1 - 25</u> is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>6, 7</u>.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
patent by another filed in the United States before the invention by the applicant for patent, except that an
international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
subsection of an application filed in the United States only if the international application designated the United
States and was published under Article 21(2) of such treaty in the English language.

2.   Claims 1, 2, 5 – 7, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by

Murade, USPN 6,531,996 B1.

Claim 1

Murade teaches a system for writing a video frame row by row in a liquid crystal display

(LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality

of rows. Murade, col. 1, lines 8 – 15. The system comprises a plurality of column switches

[TFTs 202] adapted for coupling the plurality of columns of said LCD to an output voltage; a

plurality of row switches [TFTs 30] adapted for selectively coupling the plurality of columns to

the pixels of said LCD; and logic circuitry [precharging circuit 201 with data line driving circuit

and scanning line driving circuit 104] coupled to the plurality of column switches and the

plurality of row switches. Murade, col. 12, line 47 – col. 13, line 42; and figures 1 & 12. The

logic circuitry is adapted to send a control signal [precharging circuit driving signal NRG] to the

plurality of column switches to couple said columns to a fixed voltage [precharging signal NRS]

prior to the writing of each row, thereby charging said columns prior to the writing of each row.
Murade, col. 13, lines 12 – 18 and figures 1 & 12.

Claim 2

Murade teaches that the logic circuitry includes a column control logic circuit [data line driving circuit] coupled to the plurality of column switches and a row control logic circuit [scanning line driving circuit 104] coupled to the plurality of row switches. Murade, figure 1.

Claim 5

Murade teaches a system for writing a video frame row by row in a liquid crystal display (LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality of rows. Murade, col. 1, lines 8 – 15. The system comprises a plurality of column switches [TFTs 302] adapted for coupling the plurality of columns of said LCD to an output voltage; a plurality of secondary column switches [TFTs 202] adapted for coupling at least one of the plurality of columns to a fixed voltage; a plurality of row switches [TFTs 30] adapted for selectively coupling the plurality of columns to the pixels of said LCD; and logic circuitry [precharging circuit 201 with data line driving circuit and scanning line driving circuit 104] coupled to the plurality of column switches and the plurality of row switches. Murade, col. 12, line 47 – col. 13, line 42; and figure 1. The logic circuitry is adapted to send a control signal [precharging circuit driving signal NRG] to the plurality of primary and secondary column switches to couple at least one of the plurality of columns to a fixed voltage [precharging signal NRS] prior to the writing of each row, thereby charging at least one of the plurality of columns prior to the writing of each row. Murade, col. 13, lines 12 – 18 and figure 1.

Claim 6

Murade teaches a system for writing a video frame row by row in a liquid crystal display

(LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality

of rows. Murade, col. 1, lines 8 – 15. The system comprises a plurality of column switches

[TFTs 202] adapted for coupling the plurality of columns of said LCD to an output voltage; a

plurality of row switches [TFTs 30] adapted for selectively coupling the plurality of columns to

the pixels of said LCD; and logic circuitry [precharging circuit 201 with data line driving circuit

and scanning line driving circuit 104] coupled to the plurality of column switches and the

plurality of row switches. Murade, col. 12, line 47 – col. 13, line 42; and figures 1 & 12. The

logic circuitry is adapted to send a control signal [precharging circuit driving signal NRG] to the

plurality of column switches to couple said columns to each other to thereby equalize one or

more voltages stored on the column prior to the writing of each row. Murade, col. 2, lines 56 –

67; col. 4, lines 6 – 9; col. 13, lines 40 – 67; col. 18, lines 56 – 62; and figures 1 & 12.

Claim 7

Murade teaches that the logic circuitry includes a column control logic circuit [data line

driving circuit] coupled to the plurality of column switches and a row control logic circuit

[scanning line driving circuit 104] coupled to the plurality of row switches. Murade, figure 1.

Claim 19

Murade teaches a method for writing a video frame row by row in a liquid crystal display

(LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality

of rows. Murade, col. 1, lines 8 – 15. Each column has an associated capacitor [interconnection

capacitance of a large number of data lines 35]. Murade, col. 18, lines 50 – 62; and figure 1.

Each pixel has an associated capacitor 70. Murade, col. 12, lines 61 – 64; and figure 1. Murade

teaches coupling the column capacitors together prior to writing each row, so that the voltage

stored on the column capacitors is equalized to an average value prior to writing each row.

Murade, col. 2, lines 56 – 67; col. 4, lines 6 – 9; col. 13, lines 40 – 67; col. 18, lines 56 – 62;

and figures 1 & 12.

3.   Claims 1 – 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Sekine, USPN

6,661,401 B1.

Claim 1

Sekine teaches a system for writing a video frame row by row in a liquid crystal display

(LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality

of rows. Sekine, col. 1, lines 7 – 8; and figure 2. The system comprises a plurality of column

switches [Analog Switch (ASW) TFTs] adapted for coupling the plurality of columns of said

LCD to an output voltage; a plurality of row switches [TFTs (Mpix)] adapted for selectively

coupling the plurality of columns to the pixels of said LCD; and logic circuitry [data driver

circuit and gate driver circuit] coupled to the plurality of column switches and the plurality of

row switches. Sekine, col. 5, lines 29 – 55; and figure 2. The logic circuitry is adapted to send a

control signal [Out-cnt] to the plurality of column switches to couple said columns to a fixed

voltage [V_{ps} or V_{ng}] prior to the writing of each row, thereby charging said columns prior to

the writing of each row. Sekine, col. 5, line 57 – col. 6, line 18; and figure 3.

Claim 2

Sekine teaches that the logic circuitry includes a column control logic circuit [data driver circuit] coupled to the plurality of column switches and a row control logic circuit [gate driver circuit] coupled to the plurality of row switches. Sekine, figure 2.

Claim 3

Sekine teaches that the logic circuitry is coupled to at least one digital-to-analog converter (DAC) [16R-16B], which outputs the output voltage, and said logic circuitry commands said at least one DAC to output a desired video voltage. Sekine, col. 5, line 57 – col. 6, line 18; and figures 1 & 3.

Claim 4

Sekine teaches that the logic circuitry commands said at least one DAC to output the fixed voltage. Sekine, col. 3, lines 26 – 35; col. 6, lines 7 – 18; and figures 1 & 3.

4.   Claims 8 - 12, 15 – 18, and 20 – 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Jung, USPN 6,731,266 B1.

Claim 8

Jung teaches a system for writing a video frame in a liquid crystal display (LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality of rows. Jung, col. 1, lines 7 – 11. The system comprises a plurality of primary column switches [image signal select switch blocks 320] adapted for coupling the plurality of columns of said LCD to an output voltage and a plurality of secondary column switches [precharging signal select-switch block 340] adapted for coupling at least one of the plurality of columns of said LCD to a fixed voltage

[precharging signals PC]. Jung, col. 6, line 54 – col. 7, lines 14; and figure 4. A plurality of row switches [TFT 2] are adapted for selectively coupling the plurality of columns to the pixels of said LCD. Jung, col. 1, lines 25 – 40. See also Jung, col. 10, lines 37 – 65; and figure 11 for details of the gate array. Jung describes the logic circuitry coupled to the plurality of primary and secondary column switches and the plurality of row switches. The logic circuitry is adapted to send a control signal to one primary column switch to couple its associated column to a desired video voltage and another control signal to a secondary column switch in a successive column so as to couple the successive column to the fixed voltage to thereby charge said successive column while the preceding column is being charged to the desired video voltage. Jung, col. 7, lines 15 – 33; col. 9, lines 30 – 44; and figure 9.

Claim 9

Jung teaches that the logic circuitry includes a column control logic circuit [data driver] coupled to the plurality of primary and secondary column switches and a row control logic circuit [gate driver] coupled to the plurality of row switches. Jung, col. 6, line 54 –col. 7, line 14; and col. 10, lines 37 – 65.

Claim 10

Jung teaches that the logic circuitry is adapted to send a control signal [BSn+1] to the secondary column switches [precharging signal select switch block 360] in the successive two or more columns [ny+1....ny+4] to couple said two or more successive columns to the fixed voltage PC while the preceding column [(n-1)y+4] is being charged to the desired video voltage [SIG4]. Jung, col. 7, lines 15 – 33; and figure 5.

Claim 11

Jung teaches that the logic circuitry is adapted to send a control signal [BSn] to the primary column switch [image signal select switch block 350n] to couple the successive column [ny+4] to a desired video voltage [SIG4] and send a control signal [BSn+1] to a secondary column switch [precharging signal select switch block 360n+1] corresponding to the next successive column [ny+1] to couple said next successive column to the fixed voltage PC, so that as the successive column is being charged to its desired video voltage the next successive column is being charged to the fixed voltage. Jung, col. 7, lines 15 – 33; col. 7, line 40 – col. 8, line 5; and figure 5.

Claim 12

Jung teaches that the logic circuitry is adapted to send control signals to the primary and secondary column switches and the row switches so that the sequence of charging one column capacitor to a desired video voltage while the successive column capacitor is being charged to a fixed voltage is repeated until all of the pixels in a given row have been written, and said sequence is again repeated for each successive row until all of the rows in the matrix have been written. Jung, lines 30 – 44; and figure 9.

Claim 15

Jung teaches that the fixed voltage PC is generated by a voltage supply precharging signal generator 400] independent from the voltage supply [image signal processor] that generates the desired video voltage [SIG1....SIGn]. Jung, col. 6, line 54 – col. 7, line 39; and figure 4.

Claim 16

Jung teaches a method for writing a video frame row by row in a liquid crystal display (LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality of rows. Jung, col. 1, lines 7 – 11. Each column has an associated parasitic capacitance. Jung, col. 1, line 66 – col. 2, line 5. Each pixel has an associated capacitor. Jung, col. 1, lines 25 – 40; and figure 1. Jung teaches of charging the column lines to a fixed voltage prior to writing each row. Jung, col. 2, lines 40 – 53.

Claim 17

Jung teaches that the column capacitors are charged to a fixed voltage by coupling them to an analog voltage driven to a selected preferred voltage under the command of a logic circuit. Jung, col. 7, lines 15 – 33; col. 9, lines 30 – 44; and figure 9.

Claim 18

Jung teaches that the column capacitors are charged to a fixed voltage by coupling them to a voltage supply driven to a selected preferred voltage. Jung, col. 7, lines 15 – 33; col. 9, lines 30 – 44; and figure 9.

Claim 20

Jung teaches a method for writing a video frame row by row in a liquid crystal display (LCD) having a matrix of liquid crystal pixels arranged in a plurality of columns and a plurality of rows. Jung, col. 1, lines 7 – 11. Each column has an associated parasitic capacitance. Jung, col. 1, line 66 – col. 2, line 5. Each pixel has an associated capacitor. Jung, col. 1, lines 25 – 40; and figure 1. Jung teaches charging a column capacitor to a desired video voltage while

charging a successive column capacitor to a fixed voltage during the writing of each row. Jung,

col. 7, lines 15 – 33; col. 9, lines 30 – 44; and figure 9.

Claim 21

Jung teaches charging two or more successive column capacitors [ny+1....ny+4] to a

fixed voltage PC while charging the column capacitor [(n-1)y+4] to the desired video voltage

[SIG4]. Jung, col. 7, lines 15 – 33; and figure 5.

Claim 22

Jung teaches that after the successive column capacitor [ny+1] is charged to the fixed

voltage PC it is charged to a desired video voltage [SIG4] and at the same time the next

successive column capacitor is charged to the fixed voltage. Jung, col. 7, lines 15 – 33; col. 7,

line 40 – col. 8, line 5; and figure 5.

Claim 23

Jung teaches that the sequence of charging one column capacitor to a desired video

voltage while the successive column capacitor is being charged to a fixed voltage is repeated

until all of the pixels in a given row have been written, and said sequence is again repeated for

each successive row until all of the rows in the matrix have been written. Jung, lines 30 – 44;

and figure 9.

Claim 24

Jung teaches that the column capacitor is charged to the fixed voltage by coupling it to an

analog voltage driven to a selected preferred voltage under the command of a logic circuit. Jung,

col. 7, lines 15 – 33; col. 9, lines 30 – 44; and figure 9.

Claim 25

Jung teaches that the column capacitor is charged to the fixed voltage by coupling it to a

voltage supply driven to a selected preferred voltage. Jung, col. 7, lines 15 – 33; col. 9, lines 30

– 44; and figure 9.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

6.   Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jung in

view of Sekine.

Claim 13

Jung does not teach that the logic circuitry is coupled to a digital-to-analog converter

(DAC), which outputs the output voltage.

Sekine teaches that the logic circuitry is coupled to at least one digital-to-analog

converter (DAC) [16R-16B], which outputs the output voltage, and said logic circuitry

commands said at least one DAC to output a desired video voltage. Sekine, col. 5, line 57 – col.

6, line 18; and figures 1 & 3.

It would have been obvious to one of ordinary skill in the art at the time of the invention

to combine the logic circuit with the digital-to-analog converter as taught by Sekine with the

system as taught by Jung to eliminate a separate precharging circuit. Sekine invites such

combination by teaching,

> Accordingly, it is an object of the present invention to provide a drive
> circuit for driving an active matrix type liquid crystal display and a driving
> method for a liquid crystal display drive circuit, capable of improving the yield of
> production by eliminating the precharge circuit from the liquid crystal display
> panel, and of minimizing the display variation over the whole of the liquid crystal
> display panel by carrying out the precharging in a period different from the
> horizontal blanking period.

Sekine, col. 2, line 66 – col. 3, line 7.

Claim 14

Sekine teaches that the logic circuitry commands said at least one DAC to output the

fixed voltage. Sekine, col. 3, lines 26 – 35; col. 6, lines 7 – 18; and figures 1 & 3.

Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Aoki et al., USPN 6,307,681 B1; Yamashita et al., USPN 6,744,417 B1; Jinno et al.,

USPN 6,163,310; and Lebrun et al., USPN 6,359,608 B1, each teach precharging circuits.

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Leland R. Jorgensen whose telephone number is 703-305-2650.

The examiner can normally be reached on Monday through Friday, 8:00 a.m. through 3:30 p.m..

The fax phone number for the organization where this application or proceeding is

assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lrj

DENNIS-DOON CHOW
PRIMARY EXAMINER